REMARKS

In accordance with the foregoing, claims 1-26, 33-34, 36-38 and 40 are amended. Claims 1-26, 34, 36-38 and 40 are amended to overcome formalities in accordance with the Examiner's suggestions. Claim 3 is amended to overcome a formality to indicate that "a second latch circuit (is) clocked by a third clock signal, and inputting the second output signal from the first latch circuit." New claim 41 is presented. Applicants request entry and consideration of the amended and new claims.

Claims 27-32 and claim 39 are cancelled herein without prejudice or disclaimer, and Applicants request the item 4-5 rejection to be withdrawn.

Claims 1-26, 33-35, 36-38 and 41 are pending and under consideration.

ITEMS 6-7: ALLOWABLE SUBJECT MATTER

The Examiner indicates that claim 33 is allowed. (Action at page 10).

The Examiner indicates that claims 1-26, 34-38 and 40 are "objected to because of informality, but would be allowable if rewritten to overcome the objection." (Action at page 10). Applicant thanks the Examiner fro the indication of allowable subject matter.

Claims 1-26, 34, 36-38 and 40 are amended as suggested by the Examiner to overcome the objections. Claim 35 is dependent upon claim 34, as amended. Applicants request withdrawal of the objection and that claims 1-26, 34-38 and 40 be allowed.

NEW CLAIM

New claim 41 presents no new matter and is provided to afford a varying scope of protection.

New claim 41 recites a digital-analog converter circuit including " a digital circuit to perform a series of processing cycles, comprising: an input signal processing circuit clocked by a first clock signal, inputting one or more first signal(s), and performing a predetermined processing operation on the first signal(s), and outputting a first output signal; a clock generating circuit generating second and third clock signals from the first clock signal, the second clock signal being delayed relative to the first clock signal by a first preselected delay time and the third clock signal being delayed relative to the first clock signal by a second preselected delay time; a first latch circuit being switchably clocked by the second clock signal; a second latch circuit clocked by the third clock signal, wherein the first latch circuit and the second latch circuit operate between a responsive state and a non-responsive state by turns; and an analog circuit connected to said digital circuit receiving therefrom the one or more output signal(s) to produce

one or more analog signal(s) in dependence upon the one or more output signal(s)." (See, for example, pages 14-15 starting at line 30).

These features of claim 41 patentably distinguish over the cited art, and claim 41 is submitted to be allowable for the recitations therein.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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